19-2171; Rev 3; 1/05

MAXIM

16-Bit DACs with 32-Channel Sample-and-Hold Outputs

General Description

The MAX5631/MAX5632/MAX5633 are 16-bit digital-to-analog converters (DACs) with 32 sample-and-hold (SHA) outputs for applications where a high number of programmable voltages are required. These devices include a clock oscillator and a sequencer that updates the DAC with codes from an internal SRAM. No external components are required to set offset and gain.

The MAX5631/MAX5632/MAX5633 feature a -4.5V to +9.2V output voltage range. Other features include a 200µV/step resolution, with output linearity error, typically 0.005% of full-scale range (FSR). The 100kHz refresh-rate updates each SHA every 320µs, resulting in negligible output droop. Remote ground sensing allows the outputs to be referenced to the local ground of a separate device.

These devices are controlled through a 20MHz SPI™/QSPI™/MICROWIRE™-compatible 3-wire serial interface. Immediate Update Mode allows any channel's output to be updated within 20µs. Burst Mode allows multiple values to be loaded into memory in a single, high-speed data burst. All channels are updated within 330µs after data has been loaded.

Each device features an output clamp and output resistors for filtering. The MAX5631 features a 50Ω output impedance and is capable of driving up to 250pF of output capacitance. The MAX5632 features a 500Ω output impedance and is capable of driving up to 10nF of output capacitance. The MAX5633 features a 1kΩ output impedance and is capable of driving up to 10nF of output capacitance.

The MAX5631/MAX5632/MAX5633 are available in 12mm x 12mm, 64-pin TQFP, and 10mm x 10mm, 68-pin thin QFN packages.

Applications

MEMS Mirror Servo Control

Industrial Process Control

Automatic Test Equipment

Instrumentation

Pin Configurations continued at end of data sheet.

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MICROWIRE is a trademark of National Semiconductor, Corp.

Features

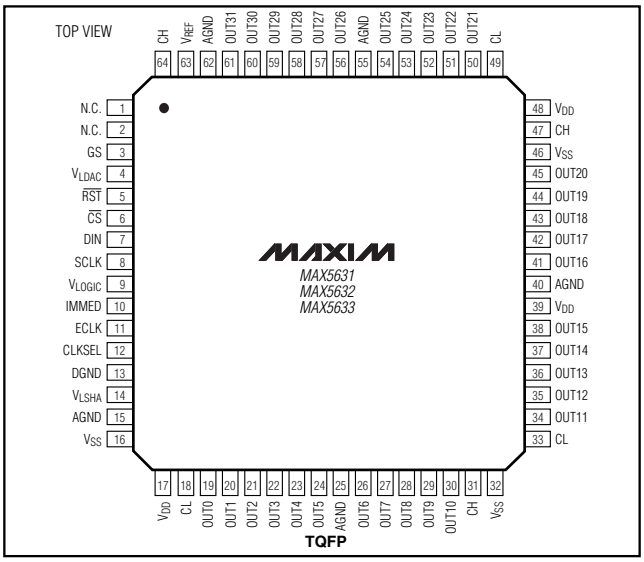
- **Integrated 16-Bit DAC and 32-Channel SHA with SRAM and Sequencer**
- **32 Voltage Outputs**
- **0.005% Output Linearity**
- **200µV Output Resolution**
- **Flexible Output Voltage Range**
- **Remote Ground Sensing**
- **Fast Sequential Loading: 1.3µs per Register**
- **Burst and Immediate Mode Addressing**
- **No External Components Required for Setting Gain and Offset**
- **Integrated Output Clamp Diodes**
- **Three Output Impedance Options: MAX5631 (50Ω), MAX5632 (500Ω), and MAX5633 (1kΩ)**

Ordering Information

PART	TEMP RANGE*	PIN-PACKAGE
MAX5631UCB	0°C to +85°C	64 TQFP
MAX5631UTK	0°C to +85°C	68 Thin QFN
MAX5632UCB	0°C to +85°C	64 TQFP
MAX5632UTK	0°C to +85°C	68 Thin QFN
MAX5633UCB	0°C to +85°C	64 TQFP
MAX5633UTK	0°C to +85°C	68 Thin QFN

**For other temperature-range options, contact factory.*

Pin Configurations



16-Bit DACs with 32-Channel Sample-and-Hold Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +12.2V
V_{SS} to AGND .....-6.0V to +0.3V
V_{DD} to V_{SS} .....+15V
V_{LDAC}, V_{LOGIC}, V_{LSHA} to AGND or DGND .....-0.3V to +6V
REF to AGND.....-0.3V to +6V
GS to AGND.....V_{SS} to V_{DD}
CL and CH to AGND.....V_{SS} to V_{DD}
Logic Inputs to DGND .....-0.3V to +6V
DGND to AGND.....-0.3V to +2V
Maximum Current Into OUT_ .....±10mA
Maximum Current Into Logic Inputs .....±20mA
Continuous Power Dissipation (T_A = +70°C)
64-Pin TQFP (derate 13.3mW/°C above +70°C) 1066mW
68-Pin QFN (derate 28.6mW/°C above +70°C) 2285mW
Operating Temperature Range.....0°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +10V, V_{SS} = -4V, V_{LOGIC} = V_{LDAC} = V_{LSHA} = +5V, V_{REF} = +2.5V, AGND = DGND = V_{GS} = 0, R_L ≥ 10MΩ, C_L = 50pF, CLKSEL = +5V, f_{ECLK} = 400kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Resolution	N		16			Bits
Output Range	$V_{OUT\_}$	(Note 1)	V_{SS} + 0.75		V_{DD} - 2.4	V
Offset Voltage		Code = 4F2C hex		±15	±200	mV
Offset Voltage Tempco				±50		µV/°C
Gain Error		(Note 2)			±1	%
Gain Tempco				±5		ppm/°C
Integral Linearity Error	INL	$V_{OUT\_}$ = -3.25V to +7.6V		0.005	0.015	%FSR
Differential Linearity Error	DNL	$V_{OUT\_}$ = -3.25V to +7.6V. Monotonicity guaranteed to 14 bits		±1	±4	LSB
Maximum Output Drive Current	I_{OUT}	Sinking and sourcing	±2			mA
DC Output Impedance	R_{OUT}	MAX5631	35	50	65	Ω
		MAX5632	350	500	650	
		MAX5633	700	1000	1300	
Maximum Capacitive Load		MAX5631		250		pF
		MAX5632		10		nF
		MAX5633		10		
DC Crosstalk		Internal oscillator enabled (Note 3)		-90		dB
Power-Supply Rejection Ratio	PSRR	Internal oscillator enabled		-80		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +10V, V_{SS} = -4V, V_{LOGIC} = V_{LDAC} = V_{LSHA} = +5V, V_{REF} = +2.5V, AGND = DGND = V_{GS} = 0, R_L ≥ 10MΩ, C_L = 50pF, CLKSEL = +5V, f_{ECLK} = 400kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Sample-and-Hold Settling		(Notes 4)			0.08	%
SCLK Feedthrough				0.5		nV-s
f_{SEQ} Feedthrough				0.5		nV-s
Hold-Step				0.25	1	mV
Droop Rate		$V_{OUT\_}$ = 0 (Note 5), T_A = +25°C		1	40	mV/s
Output Noise				250		μV_{RMS}
REFERENCE INPUT						
Input Resistance			7			kΩ
Reference Input Voltage	V_{REF}			2.5		V
GROUND SENSE INPUT						
Input Voltage Range	V_{GS}		-0.5		0.5	V
Input Bias Current	I_{GS}	-0.5 ≤ V_{GS} ≤ 0.5	-60		0	µA
GS Gain		(Note 6)	0.998	1	1.002	V/V
DIGITAL INTERFACE DC CHARACTERISTICS						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Current					±1	µA
TIMING CHARACTERISTICS (FIGURE 2)						
Sequencer Clock Frequency	f_{SEQ}	Internal oscillator	80	100	120	kHz
External Clock Frequency	f_{ECLK}	(Note 7)			440	kHz
SCLK Frequency	f_{SCLK}				20	MHz
SCLK Pulse Width High	t_{CH}		15			ns
SCLK Pulse Width Low	t_{CL}		15			ns
$\overline{CS}$ Low to SCLK High Setup Time	t_{CSSO}		15			ns
$\overline{CS}$ High to SCLK High Setup Time	t_{CSS1}		15			ns
SCLK High to $\overline{CS}$ Low Hold Time	t_{CSH0}		10			ns

16-Bit DACs with 32-Channel Sample-and-Hold Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +10V, V_{SS} = -4V, V_{LOGIC} = V_{LDAC} = V_{LSHA} = +5V, V_{REF} = +2.5V, AGND = DGND = V_{GS} = 0, R_L ≥ 10MΩ, C_L = 50pF, CLKSEL = +5V, f_{ECLK} = 400kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK High to $\overline{CS}$ High Hold Time	t_{CSH1}		0			ns
DIN to SCLK High Setup Time	t_{DS}		15			ns
DIN to SCLK High Hold Time	t_{DH}		0			ns
$\overline{RST}$ to $\overline{CS}$ Low		(Note 8)			500	µs
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	(Note 9)	8.55	10	11.6	V
Negative Supply Voltage	V_{SS}	(Note 9)	-5.25	-4	-2.75	V
Supply Difference		V_{DD} - V_{SS} (Note 9)			14.5	V
Logic Supply Voltage	V_{LOGIC}, V_{LDAC}, V_{LSHA}		4.75	5	5.25	V
Positive Supply Current	I_{DD}			32	42	mA
Negative Supply Current	I_{SS}			32	40	mA
Logic Supply Current	I_{LOGIC}	(Note 10)		1	1.5	mA
		f_{SCLK} = 20MHz (Note 11)		2	3	

Note 1: The nominal zero-scale (code = 0) voltage is -4.0535V. The nominal full-scale (code = FFFF hex) voltage is +9.0535V. The output voltage is limited by the Output Range specification, restricting the useable range of DAC codes. The nominal zero-scale voltage may be achieved when V_{SS} < -4.9V, and the nominal full-scale voltage may be achieved when V_{DD} > +11.5V.

Note 2: Gain is calculated from measurements
for voltages V_{DD} = 10V and V_{SS} = -4V at codes C000 hex and 4F2C hex,
for voltages V_{DD} = 11.6V and V_{SS} = -2.9V at codes FFFF hex and 252E hex,
for voltages V_{DD} = 9.25V and V_{SS} = -5.25V at codes D4F6 hex and 0 hex, and
for voltages V_{DD} = 8.55V and V_{SS} = -2.75V at codes C74A hex and 281C hex.

Note 3: Steady-state change in any output with an 8V change in an adjacent output.

Note 4: Settling during the first update for an 8V step. The output will settle to within the linearity specification on subsequent updates. Tested with an external sequencer clock frequency of 480kHz.

Note 5: External clock mode with the external clock not toggling.

Note 6: The output voltage is the sum of the DAC output and the voltage at GS. GS gain is measured at 4F2C hex.

Note 7: The sequencer runs at f_{SEQ} = f_{ECLK}/4. Maximum speed is limited by settling of the DAC and SHAs. Minimum speed is limited by acceptable droop and update time after a Burst Mode Update.

Note 8: V_{DD} rise to $\overline{CS}$ low = 500µs maximum.

Note 9: Guaranteed by gain-error test.

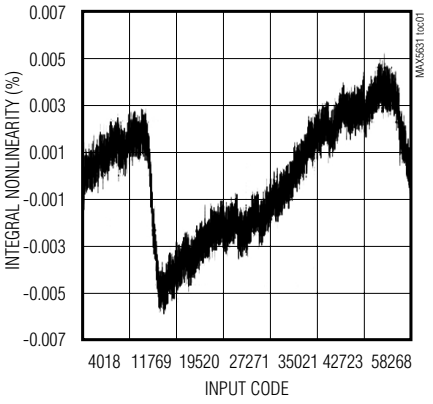
Note 10: The serial interface is inactive. V_{IH} = V_{LOGIC}, V_{IL} = 0.

Note 11: The serial interface is active. V_{IH} = V_{LOGIC}, V_{IL} = 0.

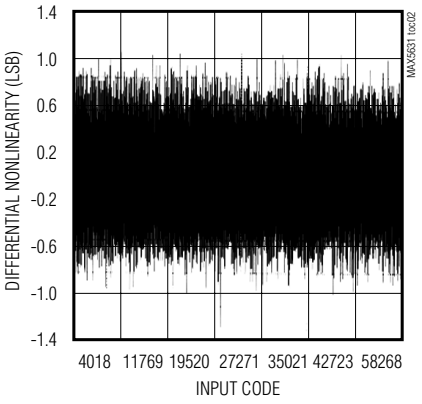
Typical Operating Characteristics

(V_{DD} = +10V, V_{SS} = -4V, V_{REF} = +2.5V, V_{GS} = 0, T_A = +25°C, unless otherwise noted.)

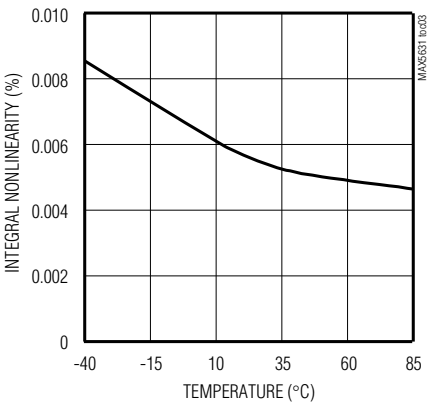
INTEGRAL NONLINEARITY vs. CODE



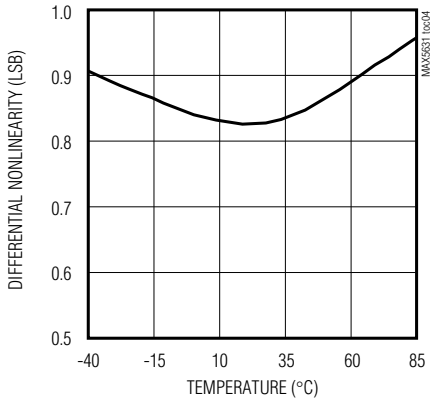
DIFFERENTIAL NONLINEARITY vs. CODE



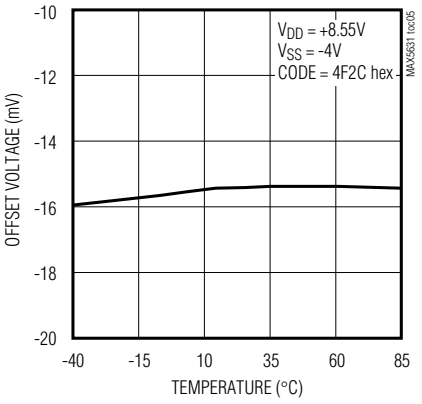
INTEGRAL NONLINEARITY vs. TEMPERATURE



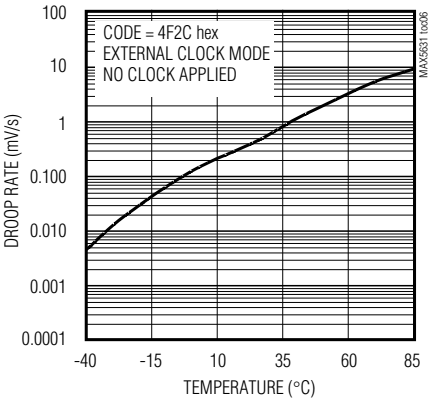
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



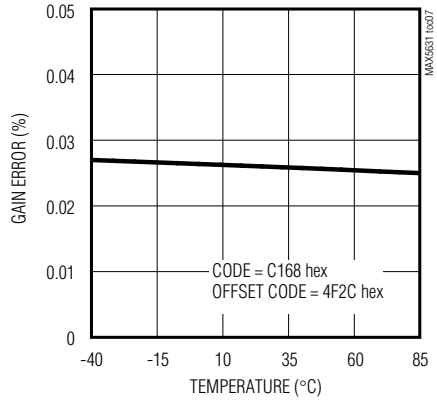
OFFSET VOLTAGE vs. TEMPERATURE



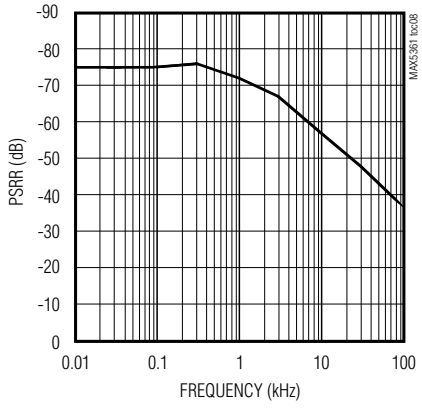
DROOP RATE vs. TEMPERATURE



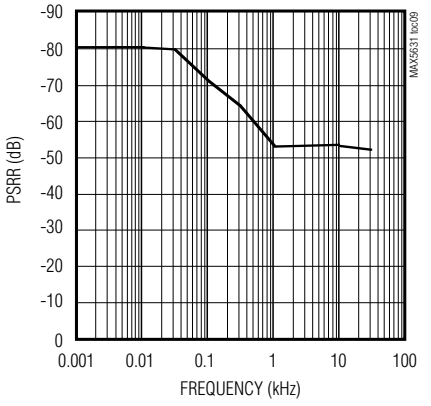
GAIN ERROR vs. TEMPERATURE



POSITIVE SUPPLY PSRR vs. FREQUENCY



NEGATIVE SUPPLY PSRR vs. FREQUENCY

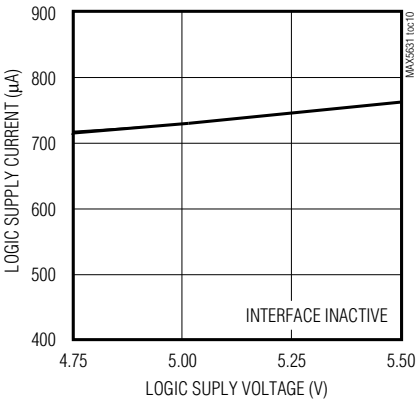


16-Bit DACs with 32-Channel Sample-and-Hold Outputs

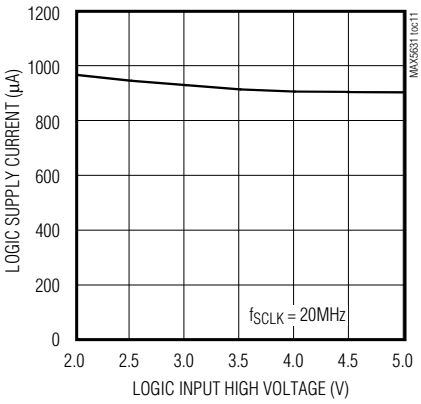
Typical Operating Characteristics (continued)

(V_{DD} = +10V, V_{SS} = -4V, V_{REF} = +2.5V, V_{GS} = 0, T_A = +25°C, unless otherwise noted.)

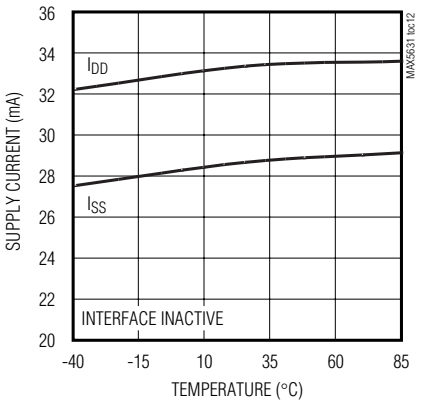
LOGIC SUPPLY CURRENT vs. LOGIC SUPPLY VOLTAGE



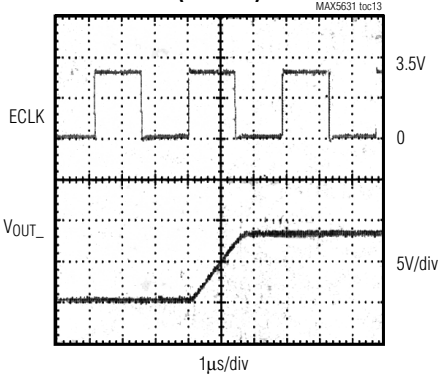
LOGIC SUPPLY CURRENT vs. LOGIC INPUT HIGH VOLTAGE



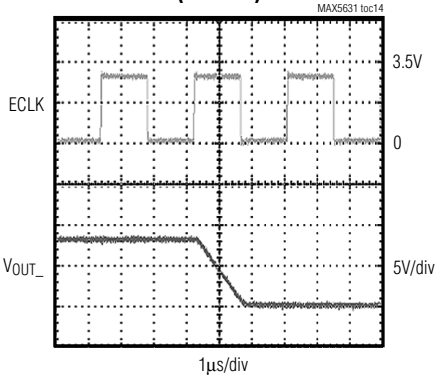
SUPPLY CURRENT vs. TEMPERATURE



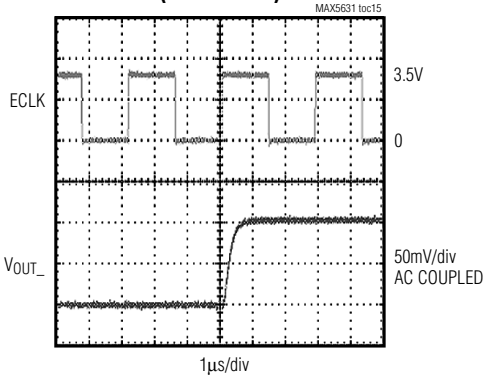
POSITIVE SETTLING TIME (8V STEP)



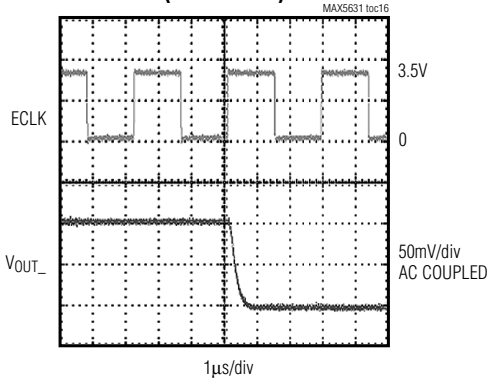
NEGATIVE SETTLING TIME (8V STEP)



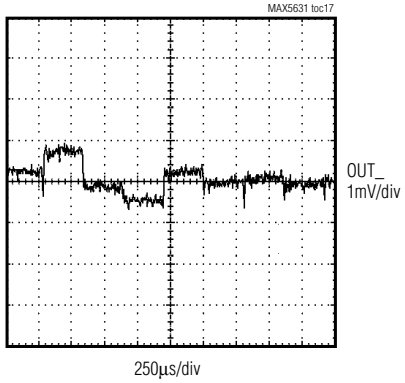
POSITIVE SETTLING TIME (100mV STEP)



NEGATIVE SETTLING TIME (100mV STEP)



OUTPUT NOISE



Pin Description

PIN		NAME	FUNCTION
TQFP	QFN		
1, 2	1, 2, 17, 34, 51, 68	N.C.	No Connection. Not internally connected.
3	3	GS	Ground-Sensing Input
4	4	V_{LDAC}	+5V DAC Power Supply
5	5	$\overline{RST}$	Reset Input
6	6	$\overline{CS}$	Chip-Select Input
7	7	DIN	Serial Data Input
8	8	SCLK	Serial Clock Input
9	9	V_{LOGIC}	+5V Logic Power Supply
10	10	IMMED	Immediate Update Mode
11	11	ECLK	External Sequencer Clock Input
12	12	CLKSEL	Clock-Select Input
13	13	DGND	Digital Ground
14	14	V_{LSHA}	+5V Sample-and-Hold Power Supply
15, 25, 40, 55, 62	15, 26, 42, 58, 65	AGND	Analog Ground
16, 32, 46	16, 33, 48	V_{SS}	Negative Power Supply
17, 39, 48	18, 41, 50	V_{DD}	Positive Power Supply
18, 33, 49	19, 35, 52	CL	Output Clamp Low Voltage
19	20	OUT0	Output 0
20	21	OUT1	Output 1
21	22	OUT2	Output 2
22	23	OUT3	Output 3
23	24	OUT4	Output 4
24	25	OUT5	Output 5
26	27	OUT6	Output 6
27	28	OUT7	Output 7
28	29	OUT8	Output 8
29	30	OUT9	Output 9
30	31	OUT10	Output 10
31, 47, 64	32, 49, 67	CH	Output Clamp High Voltage
34	36	OUT11	Output 11
35	37	OUT12	Output 12
36	38	OUT13	Output 13
37	39	OUT14	Output 14
38	40	OUT15	Output 15
41	43	OUT16	Output 16
42	44	OUT17	Output 17

16-Bit DACs with 32-Channel Sample-and-Hold Outputs

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	QFN		
43	45	OUT18	Output 18
44	46	OUT19	Output 19
45	47	OUT20	Output 20
50	53	OUT21	Output 21
51	54	OUT22	Output 22
52	55	OUT23	Output 23
53	56	OUT24	Output 24
54	57	OUT25	Output 25
56	59	OUT26	Output 26
57	60	OUT27	Output 27
58	61	OUT28	Output 28
59	62	OUT29	Output 29
60	63	OUT30	Output 30
61	64	OUT31	Output 31
63	66	REF	Reference Voltage Input

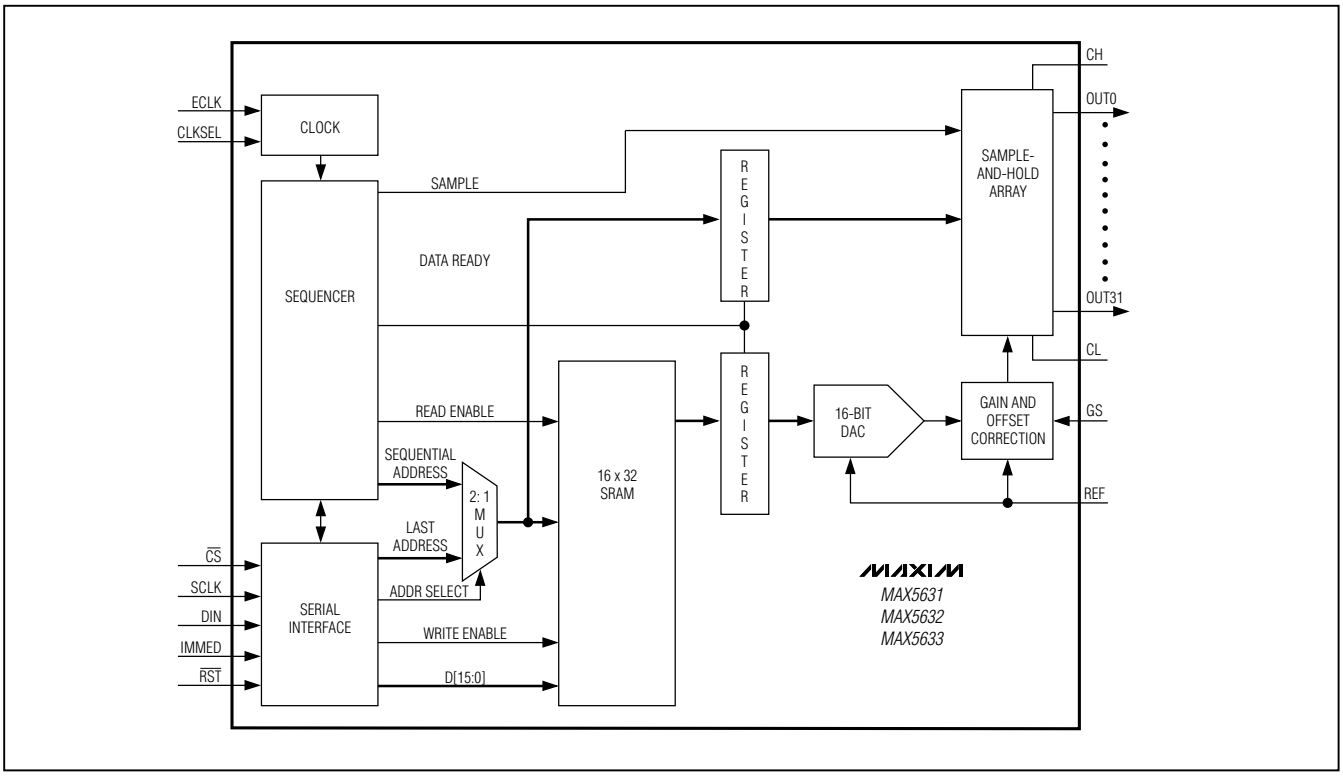


Figure 1. Functional Diagram

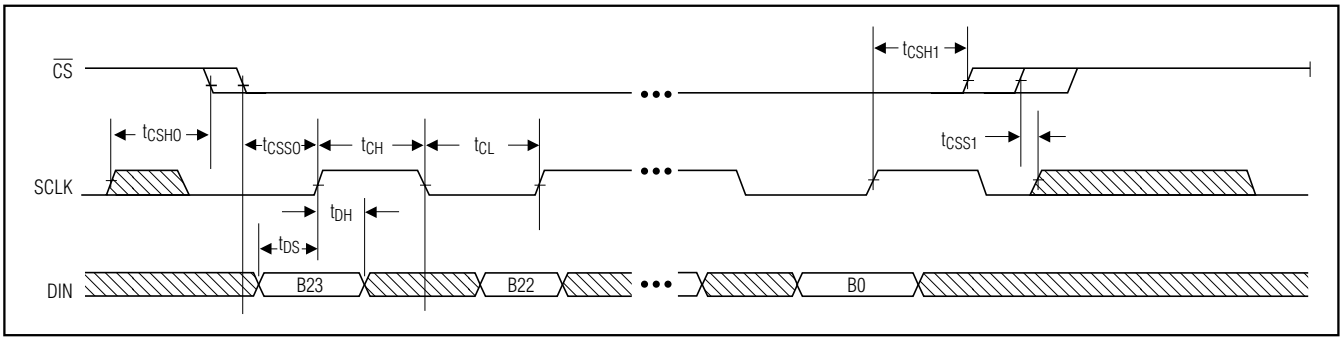


Figure 2. Serial Interface Timing Diagram

Detailed Description

Digital-to-Analog Converter

The MAX5631/MAX5632/MAX5633 16-bit digital-to-analog converters (DAC) are composed of two matched sections. The four MSBs are derived through 15 identical matched resistors and the lower 12 bits are derived through a 12-bit inverted R-2R ladder.

Sample-and-Hold Amplifiers

The MAX5631/MAX5632/MAX5633 contain 32 buffered sample/hold circuits with internal hold capacitors. Internal hold capacitors minimize leakage current, dielectric absorption, feedthrough, and required board space. MAX5631/MAX5632/MAX5633 provide a very low 1mV/s droop rate.

Output

The MAX5631/MAX5632/MAX5633 include output buffers on each channel. The device contains output resistors in series with the buffer output (Figure 3) for ease of output filtering and capacitive load driving stability.

Output loads increase the analog supply current (I_{DD} and I_{SS}). Excessively loading the outputs drastically increases power dissipation. Do not exceed the maximum power dissipation specified in the *Absolute Maximum Ratings*.

The maximum output voltage range depends on the analog supply voltages available and the output clamp voltages (see *Output Clamp*).

$$(V_{SS} + 0.75V) \le V_{OUT\_} \le (V_{DD} - 2.4V)$$

The device has a fixed theoretical output range determined by the reference voltage, gain, and midscale offset. The output voltage for a given input code is calculated with the following:

$$V_{OUT} = \left(\frac{code}{65535}\right) \times V_{REF} \times 5.2428 - (1.6214 \times V_{REF}) + V_{GS}$$

where code is the decimal value of the DAC input code, V_{REF} is the reference voltage, and V_{GS} is the

Table 1. Code Table

DAC INPUT CODE MSB LSB	NOMINAL OUTPUT VOLTAGE (V)	V_{REF} = +2.5V
1111 1111 1111 1111	9.0535	Full-scale output
1100 0111 0100 1010	6.15	Maximum output with V_{DD} = 8.55V
1000 0000 0000 0000	2.5	Midscale output
0100 1111 0010 1100	0	$V_{OUT\_}$ = 0. All outputs default to this code after power-up
0010 1000 0001 1100	-2.0	Minimum output with V_{SS} = -2.75V
0000 0000 0000 0000	-4.0535	Zero-scale output

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voltage at the ground-sense input. With a 2.5V reference, the nominal endpoints are -4.0535V and +9.0535V (Table 1). Note that these are "virtual" internal endpoint voltages and cannot be reached with all combinations of negative and positive power-supply voltages. The nominal, useable DAC endpoint codes for the selected power supplies may be calculated as:

lower endpoint code = 32768 - ((2.5V - (V_{SS} + 0.75) / 200µV) (result ≥ 0)

upper endpoint code = 32768 + ((V_{DD} - 2.4 - 2.5V) / 200µV) (result ≤ 65535)

The resistive voltage-divider formed by the output resistor (R_O) and the load impedance (R_L), scales the output voltage. Determine $V_{OUT\_}$ as follows:

$$\text{Scaling Factor} = \frac{R_L}{R_L + R_O}$$

$$V_{OUT\_} = V_{CHOLD} \times \text{scaling factor}$$

Ground Sense

The MAX5631/MAX5632/MAX5633 include a ground-sense input (GS), which allows the output voltages to be referenced to a remote ground. The voltage at GS is added to the output voltage with unity gain. Note that the resulting output voltage must be within the valid output voltage range set by the power supplies.

Output Clamp

The MAX5631/MAX5632/MAX5633 clamps the output between two externally applied voltages. Internal diodes at each channel restrict the output voltage to:

$$(V_{CH} + 0.7V) \geq V_{OUT\_} \geq (V_{CL} - 0.7V)$$

The clamping diodes allow the MAX5631/MAX5632/MAX5633 to drive devices with restricted input ranges. The diodes also allow the outputs to be clamped during power-up or fault conditions. To disable output clamping, connect CH to V_{DD} and CL to V_{SS}, setting the clamping voltages beyond the maximum output voltage range.

Serial Interface

The MAX5631/MAX5632/MAX5633 are controlled by an SPI, QSPI, and MICROWIRE-compatible 3-wire interface. Serial data is clocked into the 24-bit shift register in an MSB-first format, with the 16-bit DAC data preceding the 5-bit SRAM address, 2-bit control, and a fill 0 (Figure 4). The input word is framed by $\overline{CS}$. The first

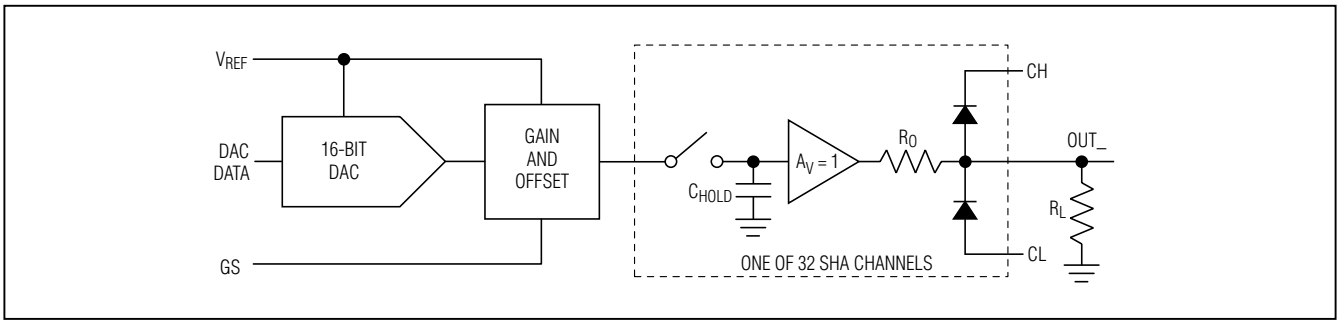


Figure 3. Analog Block Diagram

DATA																ADDRESS					CONTROL		
D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D0	A4	A3	A2	A1	A0	C1	C0	0
MSB																							**LSB**

Figure 4. Input Word Sequence

Table 2. Channel/Output Selection

A4	A3	A2	A1	A0	OUTPUT
0	0	0	0	0	OUT0 selected
0	0	0	0	1	OUT1 selected
0	0	0	1	0	OUT2 selected
0	0	0	1	1	OUT3 selected
0	0	1	0	0	OUT4 selected
0	0	1	0	1	OUT5 selected
0	0	1	1	0	OUT6 selected
0	0	1	1	1	OUT7 selected
0	1	0	0	0	OUT8 selected
0	1	0	0	1	OUT9 selected
0	1	0	1	0	OUT10 selected
0	1	0	1	1	OUT11 selected
0	1	1	0	0	OUT12 selected
0	1	1	0	1	OUT13 selected
0	1	1	1	0	OUT14 selected
0	1	1	1	1	OUT15 selected
1	0	0	0	0	OUT16 selected
1	0	0	0	1	OUT17 selected
1	0	0	1	0	OUT18 selected
1	0	0	1	1	OUT19 selected
1	0	1	0	0	OUT20 selected
1	0	1	0	1	OUT21 selected
1	0	1	1	0	OUT22 selected
1	0	1	1	1	OUT23 selected
1	1	0	0	0	OUT24 selected
1	1	0	0	1	OUT25 selected
1	1	0	1	0	OUT26 selected
1	1	0	1	1	OUT27 selected
1	1	1	0	0	OUT28 selected
1	1	1	0	1	OUT29 selected
1	1	1	1	0	OUT30 selected
1	1	1	1	1	OUT31 selected

rising edge of SCLK after $\overline{CS}$ goes low will clock in the MSB of the input word.

When each serial word is complete, the value is stored in the SRAM at the address indicated and the control bits are saved. Note that data may be corrupted if $\overline{CS}$ is not held low for an integer multiple of 24 bits.

All of the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. Their switching threshold is compatible with TTL and most CMOS logic levels.

Serial Input Data Format and Control Codes

The 24-bit serial input format, shown in Figure 4, comprises of 16 data bits (D15–D0), five address bits (A4–A0), two control bits (C1, C0), and a fill zero. The address code selects the output channel as shown in Table 2. The control code configures the device as follows:

1) If C1 = 1, Immediate Update Mode is selected. If C1 = 0, Burst Mode is selected.

2) If C0 = 0, the internal sequencer clock is selected. If C0 = 1, the external sequencer clock is selected. This must be repeated with each data word to maintain external input.

16-Bit DACs with 32-Channel Sample-and-Hold Outputs

The operating modes can also be selected externally through CLKSEL and IMMED. In the case where the control bit in the serial word and the external signal conflict, the signal that is a logic "1" is dominant.

Modes of Operation

The MAX5631/MAX5632/MAX5633 feature three modes of operation:

1) Sequence Mode

2) Immediate Update Mode

3) Burst Mode

Table 3. Update Mode

UPDATE MODE	UPDATE TIME
Immediate Update Mode	$2/f_{SEQ}$
Burst Mode	$33/f_{SEQ}$

Sequence Mode

Sequence mode is the default operating mode. The internal sequencer continuously scrolls through the SRAM, updating each of the 32 SHAs. At each SRAM address location, the stored 16-bit DAC code is loaded to the DAC. Once settled, the DAC output is acquired by the corresponding SHA. Using the internal sequencer clock, the process typically takes 320µs to update all 32 SHAs (10µs per channel). Using an external sequencer clock the update process takes 128 clock cycles (four clock cycles per channel).

Immediate Update Mode

Immediate update mode is used to change the contents of a single SRAM location, and update the corresponding SHA output. In Immediate Update Mode, the selected output is updated before the sequencer resumes operation. Select Immediate Update Mode by driving either IMMED or C1 high.

The sequencer is interrupted when $\overline{CS}$ is taken low. The input word is then stored in the proper SRAM address. The DAC conversion and SHA sample in progress are completed transparent to the serial bus activity. The SRAM location of the addressed channel is then modified with the new data. The DAC and SHA are updated with the new voltage. The sequencer then resumes scrolling at the interrupted SRAM address.

This operation can take up to two cycles of the 10µs sequencer clock. Up to one cycle is needed to allow the sequencer to complete the operation in progress before it is freed to update the new channel. An additional cycle is required to read the new data from memory, update the DAC, and strobe the sample-and-hold. The sequencer resumes scrolling from the location at which it was interrupted. Normal sequencing is suppressed while loading data, thus preventing other channels from being refreshed. Under conditions of extremely frequent Immediate Updates (i.e., 1000 successive updates), this can result in unacceptable droop.

Figure 5 shows an example of an immediate update operation. In this example, data for channel 20 is loaded while channel 7 is being refreshed. The sequencer operation is interrupted, and no other channels are refreshed as long as $\overline{CS}$ is held low. Once $\overline{CS}$ returns high, and the remainder of an f_{SEQ} period (if any) has expired, channel 20 is updated to the new data. Once channel 20 has been updated, the

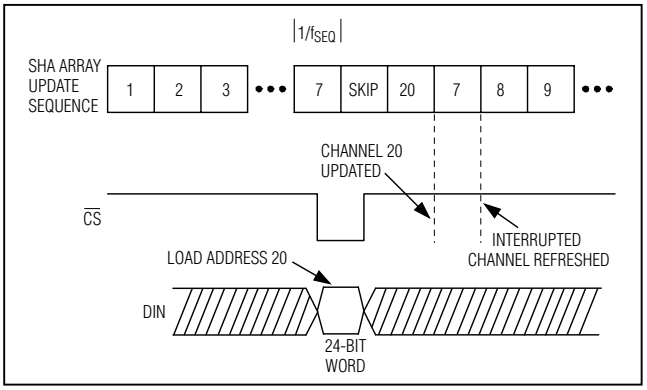


Figure 5. Immediate Update Mode Timing Example

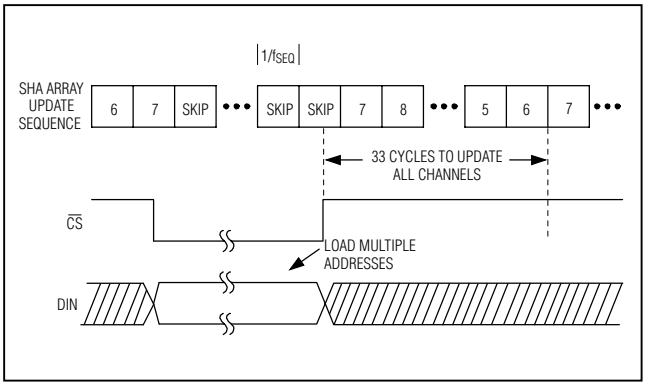


Figure 6. Burst Mode Timing Example

sequencer resumes normal operation at the interrupted channel 7.

Burst Mode

Burst Mode allows multiple SRAM locations to be loaded at high speed. During Burst Mode, the output voltages are not updated until the data burst is complete and control returns to the sequencer. Select Burst Mode by driving both IMMED and C1 low.

The sequencer is interrupted when $\overline{CS}$ is taken low. All or part of the memory can be loaded while $\overline{CS}$ is low. Each data word is loaded into its specified SRAM address. The DAC conversion and SHA sample in progress are completely transparent to the serial bus activity. When $\overline{CS}$ is taken high, the sequencer resumes scrolling at the interrupted SRAM address. New values are updated when their turn comes up in the sequence.

After Burst Mode is used, it is recommended that at least one full sequencer loop (320µs) is allowed to occur before the serial port is accessed again. This ensures that all outputs are updated before the sequencer is interrupted.

Figure 6 shows an example of a burst mode operation. As with the immediate update example, $\overline{CS}$ falls while channel 7 is being refreshed. Data for multiple channels is loaded, and no channels are refreshed as long as $\overline{CS}$ remains low. Once $\overline{CS}$ returns high, sequencing resumes with channel 7 and continues normal refresh operation. Thirty-three f_{SEQ} cycles are required before all channels have been updated.

External Sequencer Clock

An external clock may be used to control the sequencer, altering the output update rate. The sequencer runs at 1/4 the frequency of the supplied clock (ECLK). The external clock option is selected by driving either C0 or CLKSEL high.

When CLKSEL is asserted, the internal clock oscillator is disabled. This feature allows synchronizing the sequencer to other system operations, or shutting down of the sequencer altogether during high-accuracy system measurements. The low 1mV/s droop of these devices ensures that no appreciable degradation of the output voltages occurs, even during extended periods of time when the sequencer is disabled.

Power-On Reset

A power-on reset (POR) circuit sets all channels to 0V (code 4F2C hex) in sequence, requiring 320µs. This prevents damage to downstream ICs due to arbitrary reference levels being presented following system power-up. This same function is available by driving $\overline{RST}$ low. During the reset operation, the sequencer is run by the internal clock, regardless of the state of CLKSEL. The reset process cannot be interrupted, serial inputs will be ignored until the entire reset process is complete.

Applications Information

Power Supplies and Bypassing

Grounding and power-supply decoupling strongly influence device performance. Digital signals may couple through the reference input, power supplies, and ground connection. Proper grounding and layout can reduce digital feedthrough and crosstalk. At the device level, a 0.1µF capacitor is required for the V_{DD}, V_{SS}, and $V_{L\_}$ pins. They should be placed as close to the pins as possible. More substantial decoupling at the board level is recommended and is dependent on the number of devices on the board (Figure 7).

The MAX5631/MAX5632/MAX5633 have three separate +5V logic power supplies, V_{LDAC}, V_{LOGIC}, and V_{LSHA}. V_{LDAC} powers the 16-bit digital-to-analog converter, V_{LSHA} powers the control logic of the SHA array, and V_{LOGIC} powers the serial interface, sequencer, internal clock and SRAM. Additional filtering of V_{LDAC} and V_{LSHA} improves the overall performance of the device.

Chip Information

TRANSISTOR COUNT: 16,229
PROCESS: BiCMOS

16-Bit DACs with 32-Channel Sample-and-Hold Outputs

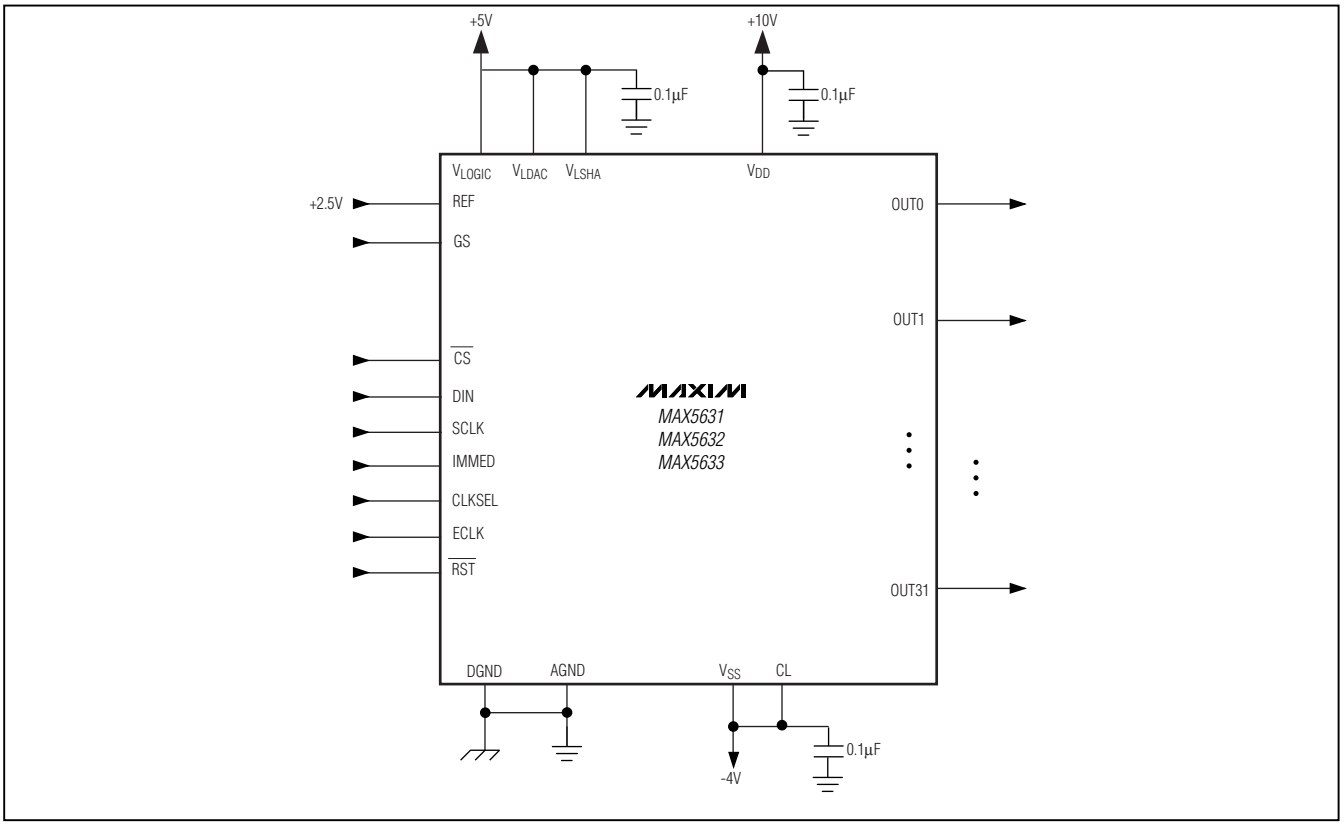
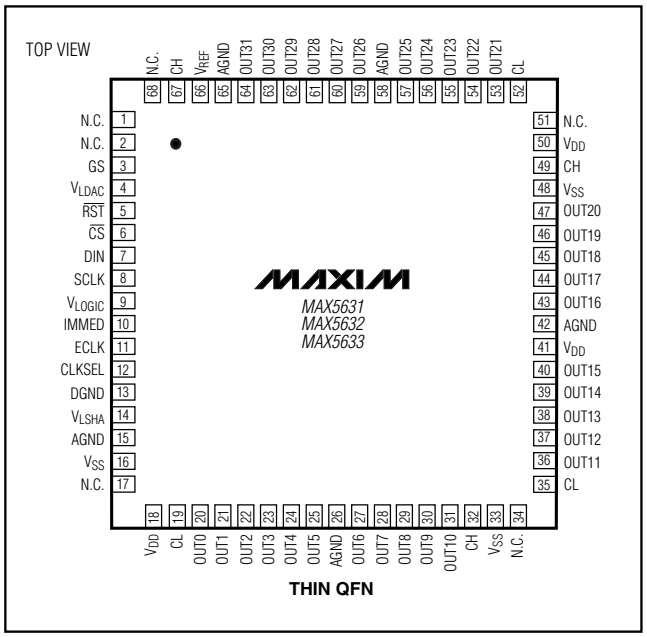


Figure 7. Typical Operating Circuit

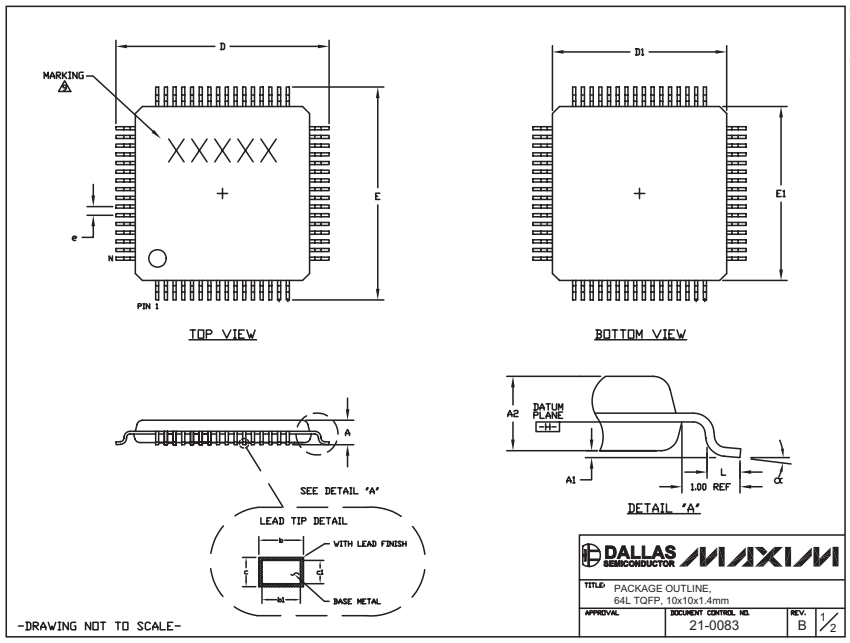
_____Pin Configurations (continued)



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

64L TQFP.EPS



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊞ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026, VARIATION BCD.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

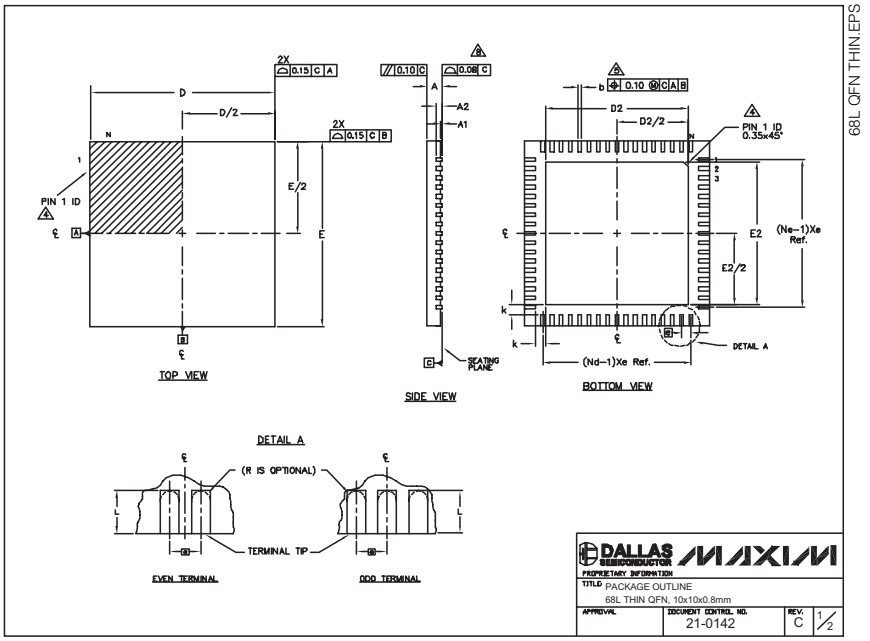
JEDEC VARIATION		
	BCD	
	64 LEAD	
	MIN.	MAX.
A	---	1.60
A_1	0.05	0.15
A_2	1.35	1.45
D	11.80	12.20
D_1	9.80	10.20
E	11.80	12.20
E_1	9.80	10.20
e	0.50 BSC.	
L	0.45	0.75
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
α	0°	7°

-DRAWING NOT TO SCALE-
DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 64L TQFP, 10x10x1.4mm
APPROVAL
DOCUMENT CONTROL NO. 21-0083
REV. B
2/2

16-Bit DACs with 32-Channel Sample-and-Hold Outputs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



PKG	68L 10x10			NOTE
REF.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
A1	0.00	0.01	0.05	
A2		0.20 REF		
b	0.20	0.25	0.30	
D	9.90	10.00	10.10	
E	9.90	10.00	10.10	
e		0.50 BSC.		
k	0.25	-	-	
L	0.45	0.55	0.65	
N		68		
ND		17		
NE		17		
JEDEC		WNND-2		

EXPOSED PAD VARIATIONS							
PKG. CODE	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T6800-1	7.60	7.70	7.80	7.60	7.70	7.80	NO
T6800-2	7.60	7.70	7.80	7.60	7.70	7.80	YES
T6800-3	7.60	7.70	7.80	7.60	7.70	7.80	NO
T6800-4	7.60	7.70	7.80	7.60	7.70	7.80	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO-220.
10. WARPAGE SHALL NOT EXCEED 0.10mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
68L THIN QFN, 10x10x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0142
REV. C
2/2